Remarks

This Amendment is in response to the Office Action dated October 31, 2005. Claims 1-41, 104-144 are pending. Claims 42-103 are withdrawn. Claims 24, 25, 28-35, 126-127, and 130-137 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1-23, 26, 27, 36-41, 104-125, 128, 129, and 138-144 are rejected. Claims 24, 25, 28-32, 126, 127, 130-134 are amended to rewrite them in independent form. Claims 33-35 are dependent on claim 32 as original. Claims 135-137 are dependent on Claim 134 as original. Claim 1 and 104 are amended. Accordingly, claims 1-41 and 104-144 remain pending in the present application.

Claims Rejections-35 USC 102(b)

Claims 1-23, 26, 27, 36-41,104-125, 128, 129, and 138-144 are rejected under 35 U.S.C. 102(b) as being anticipated by Agahi et. al., U.S.P. No. 5,559,912. Examiner stated:

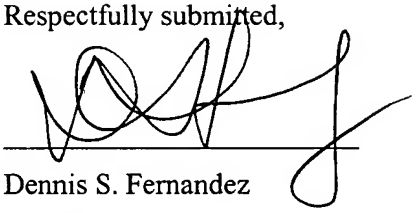
Agahi et. al. 912' teaches (Fig.1-5) an integrated photonic-electronic circuit device or wavelength processor comprising: an electronic circuit portion including plural light detectors/wavelength filters (Note that the detectors can be used for wavelength filtering, multiplexing (add/drop), broadband or narrowband coupling and can be either used with analog, RF or digital signals) 400 comprising at least one group IV semiconductor layer (silicon, germanium) and a photonic interface integrated optical waveguide coupler 106, 104 (Note that at least one waveguide can be optical fiber 300, 302) wherein the photonic interface can include SIO2 (silica) which can be at least partially transparent to light and have a bandgap energy less than that of silicon wherein all the components are formed on a silicon or SOI substrate 100 and form an integrated "chip" device.

Applicants respectfully disagree as to the claim 1 and 104 as amended. The present invention as recited in amended independent claim 1 and 104, provides an integrated photonic-electronic circuit comprising a transistor logic module in an electronic circuit portion (see Fig. 1) and a photonic interface integrated on a single chip. In contrast, what Agahi et. al. 912' presented is a planar semiconductor waveguide on a SOI substrate that the electronic circuit portion is limited to a light detector using p-n junction that is set to analyze the photo-generated carrier for wavelength selective detection. For this reason, Agahi et. al. 912' does not teach or suggest an integrated photonic-electronic circuit in a single chip as recited in amended independent claim 1 and 104. Applicant further submits that dependent claims 2-23, 26, 27, 36-41, 105-125, 128, 129, and 138-144 are allowable because they depend upon the allowable base claim 1 and 104.

Conclusion

Applicants respectfully submit that claims 1-41 and 104-144 are in condition for allowance, and thus, reconsideration of the rejections is requested. Claims 42-103 are still withdrawn from consideration as elected in last Office Action Response filed on October 3, 2005.

Respectfully submitted,



Dennis S. Fernandez

Reg. No. 34,160

Date: 4/17/06

Address: **FERNANDEZ & ASSOCIATES LLP**
1047 El Camino Real
Menlo Park, CA 94025

Customer No: **22877**

Phone: (650) 325-4999
Fax: (650) 325-1203
Email: *iploft@iploft.com*